SKAMP Correlator

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Molonglo, 16 September 2009
Basic Design

• **FX Correlator**
  • Filterbank
  • Then cross correlation
    • Each cross correlation unit operates on a subset of the frequency channels
    • Cross connect of all inputs required
    • Processing independent of frequency resolution

• **Filterbank**
  • One mode – reduces firmware development
  • Full frequency resolution across full band
  • Not possible in a single step within FPGA
    • Coarse and fine filterbank

• **Two boards**
  • PFB does filterbank and cross connection
  • Correlator does correlation and long term accumulation LTA
PFB board

Coarse Filterbank

Cross connection

Fine Filterbank

Ludi de Souza
Coarse Filterbank

- **100MHz of input bandwidth broken up into 128 frequency channels**
  - Spacing 0.78MHz
- **But sample rate 0.926MHz (Complex data)**
  - Data oversampled
  - No degradation or aliasing within 0.78MHz
Cross Connect and Fine filterbank

- Keep 120 channels from each of the 16 inputs
- Backplane connection 10 channels for 16 inputs to each PFB card
- PFB card has 10 channels for 192 inputs from backplane
- Implement 64 channel fine filterbank on each coarse channel
- Keep central 780kHz = 54 channels

- Total channels 120 x 54 = 6480 channels
- Frequency resolution = 14.4kHz
- Total Bandwidth = 93.375MHz
- Reduce resolution by averaging channels
System Connections

- 12 Processing boards per card cage
- 2 sets of PFB total 24 boards
- 2 sets of Correlators total 24 boards
- Data from PFB split between two correlator boards
• Correlator cards not interconnected, input 4 1X Infiniband
Correlator RTM to FX20

- **Input – Two 1X Infiniband connectors from a PFB in each card cage**
  - Each 1X Infiniband carries two 1.6Gbit/s signal
    - 192 antennas for 1/48 of bandwidth (2MHz)
    - Dual 1X gives 192 inputs for 1/24 of bandwidth from 1 PFB
- **Same data from second PFB gives up to 384 inputs**
Correlation Engine

- **Processes 1 MHz**
- **Four per board = 4MHz per board**
- **Correlation FPGA**
  - Totally devoted to correlation cells
  - Process one fine filterbank channel at a time
  - Average of 512 to LTA DRAM
- **Limit to 368 inputs (354 from antennas an 16 for RFI)**

- **67,528 correlation per channel, includes auto**
Output

- 30 Second accumulation to LTA DRAM.
- DRAM readout rate of final data very low.
- Use single Ethernet
  - MWA use all four
- Formats into approximately UDP blocks
  - Not fully standard compliant

- 67,528 correlation x 6480 channels
- Give 437,581,440 correlations
- 14.6M correlations/second
Board Status

- Board schematics version 1, CSIRO, Domain 42
- Routing, manufacture, testing and version 2 CSIRO
- PFB
  - Two version 1 boards built
  - Four version 2 in production
- Correlator
  - Two version 1 boards built
  - Four version 2 in production
- Slot 1 hub
  - Two version 1 boards built
  - Two version 2 in production
- PFB RTM (optical interface) Tested at speed
- Correlator RTM (passive) Test at speed
- Sign off on version 2 board – then full production run
Firmware Status

- **PFB (Ludi de Souza)**
  - Firmware written, tested in simulation
  - Firmware resource usage very comfortably within supplied resources
  - Optical links fully working
  - MWA firmware (more demanding) delivered, fully operational for 512T

- **Correlator**
  - MIT to deliver ...
  - Now uses Ludi de Souza’s Monitor/Control

- **Slot 1 hub (Ludi de Souza)**
  - Complete and working on version 1 board
Questions
PFB Data flow

RTM – 16 Multimode Optical inputs

½ FX60 - optical interface

2 Xilinx SX35 - Coarse filterbank +X4 Cross connect

3 FX20 - Backplane X12 cross connect

4 SX35 with DRAM – Fine Filterbank

½ FX60 with DRAM - x4 Cross connect, Data reordering

RTM – Interface to Correlator
RTM

• **Optical input 200Mbytes/s**
  - 1.6Gbits serial data stream
  - Optical to electrical conversion on RTM, 16 optical inputs
  - Transport to FX60 over zone 3 connectors

• **FX60**
  - In Virtex4 no Rocket I/O on signal processing SX parts
    - Must use FX part to receive data from antennas
    - FX60 has 16 Rocket I/O
    - Also does output, Single part needed here not two smaller
  - FX60 decodes serial data stream and recodes it as four LVDS signals, each 400Mbits/s
  - Data to two SX35
SX35 (coarse filterbank)

- Coarse filterbank breaks data up into 128 frequency channels – 8 inputs processed per SX35
- Original design process all 128 channels
  - Suggest we delete edge channels – corrupted by aliasing
  - Reduce from 128 to 120 (12 groups of 10)
- Oversampling ratio originally 8/7 increase to 32/27 or 16/13 for better out of band RFI rejection.
  - Sample rate increase up to 16/13 * 120/128 = 1.16
  - Plus increase from 8 to 12 bit data =1.5
  - Have allowed 32 in and 64 out in SX35
  - No data flow problems on this link
SX35

- **Other functions**
  - Delay equalisation at input sample rate (before filterbank)
    - 10ns Steps in delay
    - 1.5 degree slope across coarse frequency channels
  - Fringe stopping after filterbank
    - Fast update or linear (quadratic) approximation
- **Signal statistics**
  - Input signal level (rms?)
  - Filterbank levels
- **Single SX35 output data rate**
  - $1.6 \times 8 \times 1.16 \times 1.5 = 22.3$ Gbit/s
  - To be distributed across 12 boards
  - 1.86Gbit/s to each + overheads
    - **OK for Rocket I/O**
SX35 to backplane

- Require 11 Rocket I/O links to backplane
  - Across two SX35 22 needed
  - Plus connection to own board
- At the time cheapest solution was three FX20 parts each with 8 Rocket I/O
- One FX20 dedicated to each SX35 and 1 shared.
  - Rocket I/O split 8-3
- Dedicated FX30 has 8 Rocket I/O used and 3 input data paths (data path width 16 bits)
  - 16 bit path has data for 3 Rocket I/O
- Through channel
  - Varies board to board
  - If in shared FX20 extra from dedicated
  - Provided on 6 bit link FX20-FX20
Backplane to Fine filterbank

- Four SX35 fine filterbanks
- Two pairs, each pair process data from 12 boards (11 Rocket I/O from other boards plus through channel)
  - Half data from each channel to each SX35
  - 48 antennas 10 frequencies (120 frequencies over 12 boards)
- Input to SX35 12 bit by 3 each SX35
  - Total 72 bits (cf 16x4=64 bits from input SX35) data BW OK
- 1/3 of data from shared FX20 (receives ¼ via Rockets)
  - If through channels into dedicated FX20
  - Data from one board linked to shared
  - $1/3 + 1/12 = 1/4$
## Data source and input correspondence

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Fine Filterbank

- Input 48 antennas (6 boards), 10 frequencies
- Cannot store data for all on FPGA
- Store in DRAM and bring out long series (128k samples) of data for single antenna and frequency at one time
- DRAM data rate
  - input half of coarse filterbank output data rate
  - 11.2Gbit/s for input,
  - A little higher for output, start up of polyphase fine filterbank
  - Total ~23Gbit/s needed
  - Possible DRAM data rate 600MHz by 64bits 38.4Gbit/s
  - Efficiency 4 accesses every ~5 clocks gives 30.7Gbit/s OK
- Note Need two DRAM per coarse filterbank SX35 or 4 in total. Chose 4 SX35 with one DRAM each.
  - Efficient firmware check for SX25 replacement.
• Output of fine filterbank ~16bit, Correlator 4 bit.
• Scale data to 3-bit magnitude and round in SX35
  • Determine autocorrelation here to determine scaling
  • Dynamic or fixed scaling (TBD)
• Fine filterbank not oversampling
  • Discard overlap channels
  • Data reduction by ~1.2 plus factor of 3 for 12-bit to 4-bit
  • SX35 input BW to output BW ratio 3:1 thus data bandwidth OK
• Total for 4 SX35 = 12.5Gbit/s out
• Data in wrong order for correlator, 48 antennas processed one after the other – correlator needs data from all antennas together
• Data reordering need in DRAM 25Gbit/s with input, output. 30.7Gbit/s available OK
FX60 to RTM to Correlator

- Data at output of FX60 DRAM in correct order for correlator.
- 12.5Gbit/s of data
  - 8 Rockets active 1.56Gbit/s each
  - Via zone 3 to RTM
  - One Infiniband cable
  - Cables 4X to quad 1X for data distribution
  - Two 1X Infiniband to each of two correlator boards
- Four way cross connect in FX60 each Rocket carries data for 192 inputs (SX35 fine filterbank had 48)

½ FX60 with DRAM - x4 Cross connect, Data reordering

RTM – Interface to Correlator
Correlation Cells

- 352 inputs from antennas, add sixteen for RFI = 368
- Correlation cells process 256 at once  16x16
- Number of groups of 16 = 23
- Number of combinations between pairs 23x11= 253
  - Need two FPGAs with 127 correlation cells each for these
  - Target 128 – includes 3 that do correlation within group
- Need addition 20 cells for correlations with a group
- To implement in SX35 need extra 10 correlation cells or 138 per SX35.
  - This may be hard to achieve.
  - Look at implementing these 20 cells in LX25.
- Autocorrelation done on PFB only 112 out of 256 needed
  - Strategies for within group correlations with 10 modified cells.
- Outcome currently depends on MIT
• Assume all cells for 23 groups fit into 2xSX35 + LX25
• With a cell clock rate of 256 MHz process 4MHz per correlator board
  • 96MHz for 24 boards
• Lower clock rate reduced bandwidth
• Higher clock rate reduced number of boards

• What if 23 groups need more resources
  • Use three correlation engines to form most of needed correlation – use fourth correlation engine on board for missed correlations
    • Cost BW reduction to 75%
  • Or Upgrade LX25 to LX40 (or LX60) which should be able to implement up to 64 correlation cells, only need 105 correlation cells per SX35
Correlation Engine Data

- **Input to LTA same as 1X Infiniband 2x1.6Gbit/s = 3.2 Gbit/s**
  - 24 LVDS lines at 133MHz **OK**

- **Data to SX35 16 LVDS lines**
  - ~3/4 of input data to each
  - 2.4Gbits
  - 16 LVDS pairs at 150MHz **OK**

- **Return data**
  - 256 accumulation each of 512 input samples by 256 clocks per sample (clock 256MHz)
  - 128 correlation cells or a 36-bit accumulation per 4 clocks
  - Output data path 18-bit **OK**
Accumulation DRAM

- **LTA receives**
  - A 36-bit Accumulation every four clock cycles from two correlation SX35

- **For each accumulation**
  - Must read 64-bit long term accumulation from DRAM
  - Add new 36-bit value and write back to DRAM
  - Possible method
    - Block read of LTAs to buffer
    - Write previous buffer to DRAM while accumulating into new buffer

- **R/W 256 MHz**
  - 600MHz possible **OK**
  - 50% bandwidth used
Board Status (2)

- **RTMS**
  - Both being laid out for SKAMP

- **Controller**
  - Not needed initially
  - Proceed after RTMs
• **Data flow in SKMAP examined**
  • All paths have adequate bandwidth

• **Ludi to address FPGA functionality for PFB**
  • And command and control for PFB and Correlator

• **Greatest Risk**
  • Adequacy of SX35 to accommodate 127 (138) correlation cells at reasonable speed
    • MWA responsibility
    • Initial results not promising
  • LX25 replaced by LX60 promising solution

• **For boards only major uncertainty is FX60 problem**
  • Have path to fully functional prototype PFB and Correlator
  • RTMs being routed now
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