



MAKING THE MOST OF SKAMP

Delivery of the SKAMP digital system

The School of Physics and CSIRO celebrated the official handover of the SKAMP Digital System on the 10th September 2010.

The University of Sydney contracted CSIRO to assist in developing a signal-processing system to dramatically boost the performance of the existing Molonglo Observatory Synthesis Telescope (MOST) as part of its transformation to SKAMP.

The heart of the new system is based on programmable logic chip technology which has taken SKAMP to an international level of functionality by making the telescope more flexible.

MOST has only 3MHz of bandwidth, centred on 843MHz. The new digital correlator and filterbank system has increased the bandwidth to 30MHz (around the same central frequency). As a result, the telescope's sensitivity has improved by a factor of three, producing deeper images with spectral information, which is something new for this telescope. The data-flow rate has increased by an astonishing factor of 10,000.

To transform MOST into SKAMP, the University has also upgraded the telescope's mechanical drive, changed the signal receivers, and replaced copper cables with fibre optics. The University plans to further enhance the telescope with a new dual polarization feed system, which will boost the bandwidth by another factor of three, up to 100 MHz, and allow measurements of cosmic magnetic fields. The frequency range will be broadened to cover from 650 MHz to 1200 MHz.

The formal handover of the complex digital system recently took place at the University of Sydney between CSIRO SKA Director, Professor Brian Boyle, SKAMP Project Leader, Professor Anne Green, and Mr Wayne Arcus of the Murchison Widefield Array (MWA) project.



Anne Green, Duncan Campbell-Wilson, the University of Sydney and Brian Boyle, CSIRO. SKAMP Digital System Handover. Courtesy CSIRO.



SKAMP Digital System Handover. Courtesy University of Sydney



RFI shielding prototype - the beginning . Courtesy Molonglo Observatory.

STAFF ANNOUNCEMENT

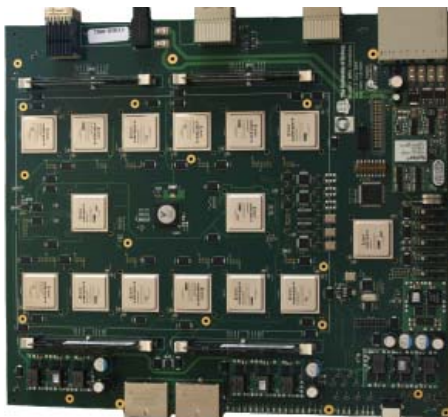
John Wills joined the Molonglo team in September, as Senior Technical Officer. He is responsible for the maintenance of the electromechanical systems and line feeds at the observatory in preparation for SKAMP.

John's mechanical engineering experience is considerable, having worked with many organisations such as Hyundai and Mitsubishi, as well as with the late Peter Brock. He has already made significant contributions to the work being done at Molonglo.

DIGITAL SYSTEM UPDATE

Polyphase Filter Bank (PFB)

Ludi de Souza reports that the SKAMP PFB firmware design is now complete with testing in silicon confirming the desired channel response. Data buffering and re-ordering, using the external DDR2 Memory (deep memory buffer) are also operating as expected, and without error. Debugging has been facilitated through the time-stamped and just-in-time packet processing architecture used throughout the design. The link infrastructure between the FPGAs & PFB boards is in place to accommodate the Full MESH interconnected multi-board system required for the complete SKAMP-2 system.



Correlator Board designed by CSIRO for the SKAMP Digital System. Courtesy Molonglo Radio Observatory

FRONT END

RF shielding

The shielded room which will house the digital system is now complete, with 4 ATCA chassis, cooling fans, power supplies and cabling.

To better isolate the control building as a whole from the telescope, metal sheeting is currently being installed around the building. The construction is being undertaken by John Wills.

Data Pipeline Network

The network within the room is also in place with fibre optic connectivity to the outside world and 3 sub-networks set up to quarantine control, correlator and outside traffic with the help of two 48-port and two 16-port switches.

Receiver

The final prototype of the Downconverter board is now complete and the FPGA Digitiser board is almost to production readiness. Duncan Campbell-Wilson and Lindsay Harkness are resolving the penultimate issues in the design of both boards before production in November 2010.

Correlator

Darshan Thakkar and Ludi de Souza have successfully instantiated the required number of correlation cells for the complete SKAMP-2 system (138 per CMAC FPGA), while exceeding the desired frequency of operation (256 MHz) and maintaining an optimum device utilisation (around 60%). This ensures that the 24 SKAMP correlator boards can process the whole bandwidth for all antennas.

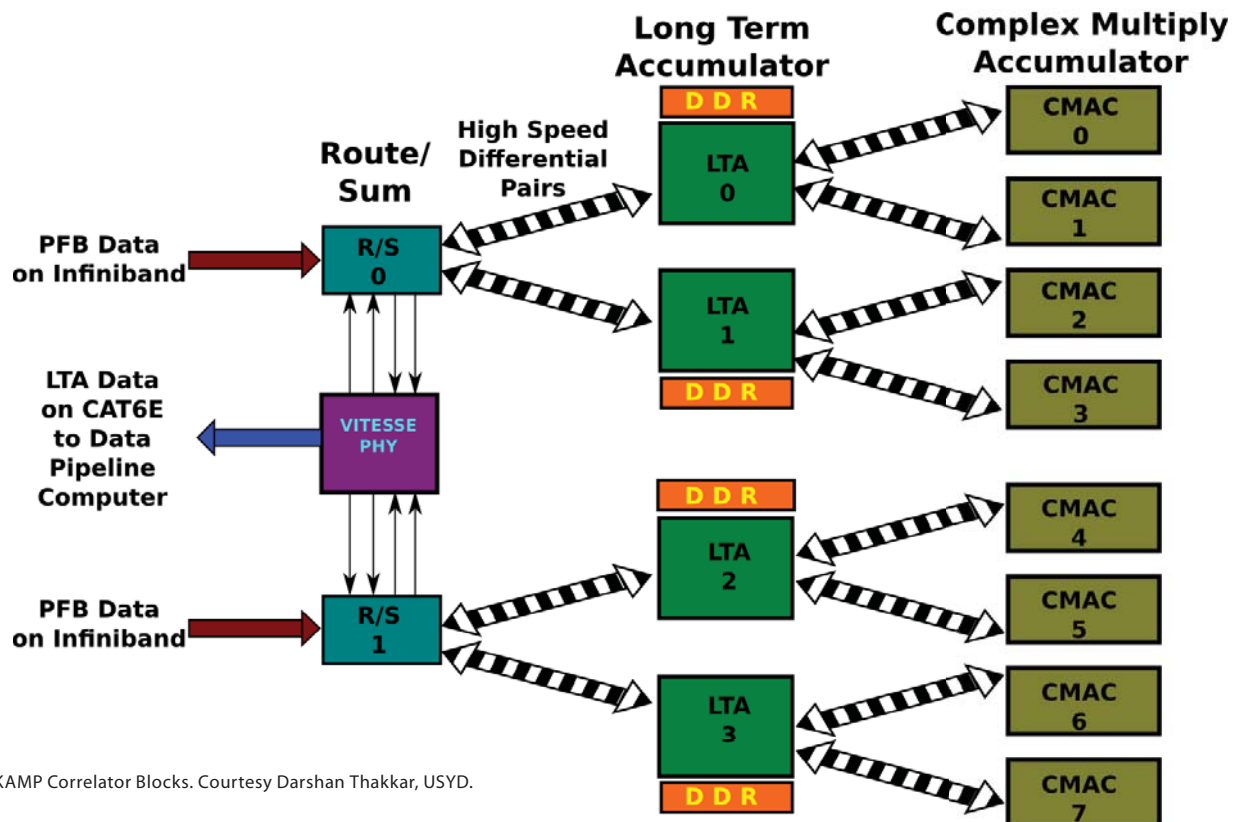
Initial testing of the data flow control system along with the cells in silicon is showing promising results and a functional test is in progress.

Future correlator development includes:

- Implementation of the required glue logic to complete the forward path, i.e. passing the PFB data through the R/S and LTA chips to the cells in the required format
- Output path development incorporating the long term accumulation (32 sec) using the external DDR memory
- Implementation of the Gigabit Ethernet Controller and its peripheral logic to facilitate dumping of correlated data to the Data Pipeline computer.

SKAMP Correlator block diagram on the next page.

SKAMP Correlator Blocks



SKAMP Correlator Blocks. Courtesy Darshan Thakkar, USYD.

SKAMP Correlator Board FPGA Functions

- **Route/Sum (R/S) FPGAs**
 1. collect PFB data forward it to the correlation cells in the CMAC FPGA via the LTA FPGA
 2. sent the long-term accumulated data to the Data Pipeline Computer via the on-board ethernet PHY using a Gigabit Ethernet Media Access Controller core
- **Long Term Accumulator (LTA) FPGAs**
 1. decode/format/re-frame the PFB data for processing by the CMAC correlation cells
 2. read cell output data from CMAC and accumulate it over the desired duration by using the DDR memory
 3. forward the long-term accumulated data from DDR to the Route/Sum FPGA
- **Complex Multiply Accumulator (CMAC) FPGAs**
 1. process the PFB data using 138 correlation cells
 2. generate appropriate control signals for the cells to ensure desired read/write operation
 3. read data from cells and send them to the LTA FPGA.

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SKAMP Newsletter

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