Single-electron transistor coupled to a silicon nano-MOSFET

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ABSTRACT

By capactively coupling sensitive charge detectors (i.e. single-electron transistors - SETs) to nanostructures such as quantum dots and two-dimensional systems, it is possible to investigate charge transport properties in extremely low conduction regimes where direct transport measurements are increasingly difficult. Ion-implanted nano-MOSFETs coupled to aluminium SETs have been constructed in order to study charge transport between locally doped regions in Si at mK temperatures. This configuration allows for direct source-drain measurement as well as non-invasive charge detection. Of particular interest are the effects of material defects and gate control on charge transport, which is of relevance to Si-based quantum computing.

1. INTRODUCTION

There has been extensive research into understanding the properties of nanostructures such as quantum dots and two-dimensional electron systems by direct transport measurements. Source-drain leads allow these systems to be probed by electrical measurement of current enabling the observation of properties such as the quantum Hall effect [1] and the atom-like shell structure of quantum dots [2 - 4]. However, direct current measurements are limited by amplifiers which typically enable currents to be measured down to the pico-amperes. An alternative approach to extend transport studies into low current regimes, below the limit of current amplifiers, is to use sensitive electrometers such as single-electron transistors (SETs) [5, 6]. SETs are extremely sensitive charge detectors capable of detecting fractions of an electron changes in their local electrostatic environment [7, 8]. One motivation for using SETs to investigate charge transport in nanostructures is solid-state quantum computing. For example, the silicon-based quantum computer proposed by Kane [9, 10] incorporates an array of single phosphorus donors embedded in a silicon crystal. For a spin-based quantum computer, the state of the quantum bit (qubit) is given by the phosphorus nuclear spin. The proposed readout scheme involves a spin dependent charge transfer process between adjacent donors. Thus charge transport between locally doped regions in silicon at milliKelvin temperatures is of particular interest.

We use SETs as charge detectors due to their high charge sensitivities. Charge sensitivities of $4.4 \times 10^{-6} \, e / \sqrt{\text{Hz}}$ [11] have been reported, close to the theoretical quantum limit of $\sim10^{-6} \, e / \sqrt{\text{Hz}}$ [12]. An SET consists of a small metallic island connected to source and drain leads by tunnel junctions. The SET island has a characteristic charging energy due to Coulomb repulsion of electrons on the island. This energy is determined by the island capacitance to its environment, given by $E_C = e^2 / 2C$, and defines the spacing of the energy levels on the island. Thus, for an additional electron to occupy the island it must overcome this charging energy. For current to flow across the SET the Fermi levels of the source and drain must be aligned to the energy levels on the island. Sweeping a voltage on a gate that is capacitively coupled to the SET can change the island electrostatic potential and move the island energy levels through the Fermi level. Single electrons can then tunnel from source to island to drain of the SET resulting in periodic conductance oscillations known as Coulomb blockade oscillations. Single-electron tunneling is a quantum mechanical process whereby the wave-like nature of electrons allows them to penetrate a classically forbidden region of space, in the case of an SET the potential barrier of the tunnel junctions. To observe electron tunneling effects the resistance of the tunnel junctions must be greater than the resistance quantum $\hbar / e^2$, and the SET must be operated at cryogenic temperatures where the thermal energy is significantly smaller than the charge energy ($k_B T \ll E_C$). By using a gate to bias the SET to a point of high transconductance the SET can be operated as a very sensitive electrometer in which extremely small changes in the local electrostatic environment lead to significant change in the SET output.
Nano-MOSFETs are an ideal device for investigating charge transport between locally doped regions in silicon. By using standard direct current measurements, valuable information can be obtained about the gate control of the conducting channel, as well as materials issues such as the effects of Si/SiO$_2$ interface traps and other defects [13]. To extend charge transport investigation into the low current regime an SET can be coupled to the channel of a nano-MOSFET. Figure 1 shows a schematic of such a device. The nano-scale source and drain leads of the MOSFET are defined by electron-beam lithography and phosphorus ion implantation. Electrical contact to the source-drain leads are via phosphorus diffused ohmics. The surface SET is fabricated using a shadow evaporation technique [14] and is positioned directly on top of the MOSFET channel. The SET operates as the MOSFET gate as well as a charge detector coupled to the channel. The combination of direct current measurements together with charge sensing by the surface SET can potentially yield information about the physical structure of the defects in the nominally intrinsic barrier between the locally doped source and drain leads. This paper will focus on the device fabrication and initial characterisation measurements using direct current measurement techniques.

![Schematic of a nano-MOSFET with implanted phosphorus source-drain leads for direct current measurement and surface SET for charge detection measurement.](image)

2. DEVICE FABRICATION

Standard microfabrication is used to fabricate the device ohmics. Taking a nominally intrinsic n-type silicon wafer (>5kΩ.cm) a field oxide is thermally grown. Optical lithography and a hydrofluoric (HF) acid etch of the field oxide define a diffusion mask and a phosphorus diffusion step creates the ohmics. In the final micro-processing stage another optical lithography step and HF etch define a thin oxide region between the ohmics and a high quality 5nm gate oxide is grown using a triple walled furnace to provide higher oxide qualities. Electrical characterisation measurements of 5nm gate oxide grown in this furnace indicate trap densities of $2 \times 10^{11}$ cm$^{-2}$ at 4.2K [13].

After microfabrication of the ohmic contacts, high-resolution alignment marks, approximately 100nm x 100nm, are created by electron-beam lithography (EBL) and titanium-platinum (15nm Ti, 65nm Pt) metallisation and lift-off. These alignment marks are used to align subsequent electron-beam lithography steps to within ± 50nm accuracy. Another EBL step is then performed to fabricate an ion implantation mask in 150nm poly-methyl-methacrylate (PMMA) resist to define the nano-MOSFET source-drain leads. In the ion implantation mask the MOSFET channel is design to be approximately 60nm wide, whilst three different channel lengths (80nm, 100nm and 150nm) were fabricated. 14kV phosphorus ions are implanted with an areal dose of approximately $1.22 \times 10^{14}$ cm$^{-2}$ forming the source-drain leads. After ion implantation and removal of the PMMA mask scanning electron microscope (SEM) imaging shows a distinct contrast between the ion implanted and the masked regions (Figure 2(a)). The MOSFET channel dimensions indicated in the SEM imaging (channel width of 100nm, and channel lengths of 35nm, 50nm and 100nm) are different to the specified design and this is thought to be due secondary electron emission from
regions of ion implantation damage which is likely to extend beyond the dimensions of the ion implantation mask. A rapid thermal anneal (RTA) at 1000°C for 5 seconds is carried out to repair the implantation damage and electrically activate the phosphorus donors. After the RTA, SEM imaging of the implanted regions show significantly less contrast to the masked regions.

The SET and its gates are fabricated in two additional EBL steps accurately aligned to the ion implanted MOSFET source-drain leads. The SET gates are fabricated using a single layer 60nm PMMA resist process and TiAu (10nm Ti, 20nm Au) metallisation and lift-off. Finally the SETs themselves are fabricated using a shadow mask evaporation technique [14]. The shadow mask technique involves a bilayer resist process, in which the bottom resist layer (~500nm) is more sensitive to electron-beam exposure than the top resist layer (~60nm). The bottom resist layer is a copolymer of PMMA and methacrylic-acid (MAA) and after e-beam lithography forms a large undercut profile when developed in isopropanol: methyl-isobutyl-ketone (IPA:MIBK) 1:3. The top layer resist is PMMA and acts as a shadowing mask for subsequent evaporations. The SETs are formed by aluminium evaporation at two different angles with an in situ oxidation between the evaporations. The angle of the evaporation controls the overlaps of the two metal films and the oxidation creates the tunnel junctions. The tunnel junction capacitance is determined by the overlap area of the two metal films whilst the tunnel junction resistance for a given overlap area is controlled by the oxidation time and pressure. In the very final fabrication step, contact is made to the diffused ohmics by optical lithography, HF etch and aluminium-gold (30nm Al and 30nm Au) metallisation and lift-off. The completed device is shown in Figure 2(b) with the implanted source-drain leads highlighted schematically.

Figure 2(a) SEM image of the Si:P source-drain leads after ion implantation and before RTA. 2(b) shows an SEM image of the completed device with the implanted phosphorus leads highlighted schematically.

### 3. MEASUREMENT RESULTS

Measurements were performed at 4.2K (liquid He) and 50mK (He dilution refrigerator) using standard lock-in techniques and excitation voltages of 100-500µV. Initial experiments of the device have focused on direct current measurements to characterise the implanted nano-MOSFET with the SET being used solely as the MOSFET gate. The operation of the surface SET has been confirmed and basic characterisation has been performed but is not reported in this paper. Experimental data is presented for one device with a channel length of 150nm, although the results are characteristic of all the devices that were measured.

Basic MOSFET gate sweeps were performed at 4.2K. In Figure 3(a) the measured source-drain current of the implanted device is plotted as a function of gate bias and results show typical MOSFET behaviour. For gate voltages below 0.5V the source and drain are isolated from each other and there is no directly measurable current through the MOSFET. As the gate voltage increases above 0.5V there is a significant increase in the measured current. The increasing positive voltage is accumulating electrons under the gate gradually forming an inversion layer. Above 0.9V the inversion layer is completely formed and the source-drain current saturates. In a more detailed analysis (Figure 3(b)) of the measured current as a function of gate voltage additional features are observed that are not typical MOSFET characteristics. Small oscillations are visible in the measurements and more pronounced in the region of onset of conduction in the MOSFET. These oscillations are strongly indicative of Coulomb blockade in the channel of the MOSFET.

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Further measurements were performed at 50mK to confirm the Coulomb blockade behaviour in the MOSFET. A bias spectroscopy measurement was carried out. The source-drain bias of the MOSFET was swept from -5mV to 5mV and the gate voltage stepped from 0.5V to 0.7V. This measurement is shown in Figure 4 as an intensity plot with the MOSFET differential resistance shown ranging from high (dark) to low (light). In the plot, diamond features, commonly referred to as Coulomb diamonds, are observed indicating that the oscillations result from Coulomb blockade in the MOSFET channel. The blue regions in the plot are where the device is in Coulomb blockade regions and there is minimum current flow. Coulomb blockade in nano-MOSFETs has been previously observed [15] and is attributed to disorder in the MOSFET channel. Defects and stray dopants may create local minimum potentials in the channel which result in Coulomb blockade behaviour. Such observations give valuable information about the material issues to be faced. Disorder in the channel has a clear effect on the charge transport between the locally doped regions (source and drain leads).

Figure 3(a) Direct current measurement of nano-MOSFET $I_{SD}$ as a function of gate voltage performed at 4.2K. 3(b) A higher resolution measurement of the nano-MOSFET $I_{SD}$ showing oscillations at the onset of conduction.

As described previously, Coulomb blockade originates from the charging energy of a device and this can be determined from the width of the Coulomb diamonds. The Coulomb diamonds in the MOSFET differ from those of a metallic SET in that the width of the diamonds changes as a function of gate voltage. From Figure 4 it is observed that as gate voltage increases the width of the diamonds decreases. Such behaviour is consistent with that of GaAs quantum dots [16]. The local minimum potential, or ‘quantum dot’, created in the channel by defects and stray dopants has a small and well defined number of energy states. As gate voltage is increased the occupancy of the ‘quantum dot’ is increased by one electron at a time which in turn increases its capacitance to the environment and hence decreases its charging energy. This continues until there are no more available energy states to be occupied and then Coulomb Blockade is no longer observed. In the case of nano-MOSFETs an additional factor is the gradually forming inversion layer as the gate voltage is increased. Once a full conducting channel is formed under the gate Coulomb blockade is no longer observed.

4. CONCLUSION

We have constructed implanted Si:P nano-MOSFETs coupled to SETs for the purposes of studying charge transport between locally doped regions in silicon at mK temperatures. Direct current measurements as well as indirect charge detection can be carried out using source-drain leads and surface SETs. Initial measurements have involved direct current measurements of the nano-MOSFET and indicate that transport between the locally doped regions (source-drain leads) is affected by disorder in the channel which is observed as Coulomb blockade behaviour. The operation of the SET has been confirmed and basic characterisation carried out. Future measurements will focus on utilising...
the SET to investigate how the disorder in the channel affects transport between the source and drain leads in the low current regime.

Figure 4. Bias spectroscopy of the implanted nano-MOSFET showing Coulomb Blockade “diamonds” in di/dv as a function of $V_{SD}$ and $V_{LG}$. The charging energy of the ‘dot’ in the channel decreases as the occupancy of the dot is increased with positive gate voltage.

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T = 50mK